High frequency control of a semiconductor switch

The present invention relates to the control of a semiconductor switch, and, more specifically, to an improved operation of a resonant driver circuit for a semiconductor switch. In particular, the present invention relates to a method of operating a resonant driver circuit for driving a semiconductor switch and to a control circuit for operating a resonant driver circuit for driving a semiconductor switch.

It is known in the prior art of power converters that the kind of gate drive circuit coupled to the power MOSFET switches has a crucial influence on the efficiency of the power converter, especially at high frequencies. Thus, various driver schemes have been developed. The gate drive power loss is proportional to the switching frequency and is a major limitation in the design of high efficient power converters in the MHz region. One approach to improve the gate drive power loss is to use a resonant gate circuit as described in a paper entitled "A MOS gate drive with resonant transitions," by D. Maksimovic, 22nd Annual IEEE power electronics specialists conference (PESC), June 23 to 27, 1991, page 523 to 527. This paper describes a gate drive that provides quasi-square wave gate-to-source voltage with low impedance between gate and source terminals in both on and off states. The equivalent gate capacitance of the power MOS transistor is charged and discharged in a resonance circuit, so that energy stored in the equivalent gate capacitance is returned to the power source of the driver.

Such resonant gate drive circuits may, for example, be used in power electronics with MOSFETs that work with high switching frequencies. Thus, they may, for example, be used in switch mode power supplies (SMPS). Also, they may be adapted for applications with special requirements relating to the size, flatness, EMI or dynamics, such as voltage regulator modules (VRMs) for data processors (MPS), for flat displays and SMPS for audio sets with AM/FM tuner.

At high switching frequencies in the MHz region or higher, a both efficient and fast driving of the MOSFETs becomes more and more important. Efficient driving is necessary to reduce gate driver losses. Fast driving is necessary to keep switching losses of the power transistor inside of acceptable limits.

To achieve efficient driving, the application of resonant drivers, which are more efficient than, for example, hard switching drivers, is becoming more and more desirable. However, known resonant drivers do not achieve the same switching speed and thus are often not suitable for applications that have switching frequencies in the MHz region or higher.

It is an object of the present invention to provide for an improved operation of a resonant driver circuit for driving a semiconductor switch.

According to an exemplary embodiment of the present invention, the above object may be solved by a method, as set forth in claim 1, of operating a resonant driver circuit for driving a semiconductor switch. According to this exemplary embodiment of the present invention, the driver circuit includes a first switch for connecting a power supply via an inductor to a control terminal of the semiconductor switch and a second switch connected to the control terminal of the semiconductor switch for controlling a switching of the semiconductor switch. According to an aspect of this exemplary embodiment of the present invention, the inductor is pre-charged before a switching of the second switch.

Advantageously, due to the pre-charging of the inductor, a higher initial current may be applied to the control terminal of the semiconductor switch, thus, advantageously, both a fast and efficient switching of the semiconductor switch may be provided.

This improved operation combines both the efficient and the fast driving which are necessary for applications which have switching frequencies in the MHz region or higher.

According to an exemplary embodiment of the present invention as set forth in claim 2, an inductor current is built up previous to the switching of the second switch.

According to another exemplary embodiment of the present invention as set forth in claim 3, the inductor current before switching the second switch and thus the pre-charging of the inductor is realized by providing a time period before the switching of the second switch, during which the first switch and the second switch are switched on.

Claims 4 to 7 provide for further exemplary embodiments of the present invention. In particular, according to the exemplary embodiment of the present invention as set forth in claim 6, a method according to an exemplary embodiment of the present invention is applied to a resonant driver circuit comprising four switches and having a simple and robust set-up.

According to another exemplary embodiment of the present invention as set forth in claim 8, a control circuit is provided for operating a resonant drive circuit for driving a semiconductor switch. The control circuit according to this exemplary embodiment of the present invention comprises a switch controller for controlling the switching of the first and second switches, such that the inductor is pre-charged before a switching of the second switch.

Advantageously, this control circuit may be applied to known resonant gate driver circuits and allows for a fast and efficient operation of the semiconductor switch at high frequencies.

Claim 9 provides for an exemplary embodiment of the control circuit according to the present invention.

It may be seen as the gist of an exemplary embodiment of the present invention that the inductor of the resonant driver circuit is pre-charged before a switch controlling the switching of the semiconductor switch (such as a MOSFET) performs a switching. Due to this, an inductor current is built up, previous to the switching action, causing that an initial current charges the gate of the MOSFETs and thus allows for a faster switching of the MOSFET. According to an aspect of the present invention, the pre-charging may be performed by providing a time period, where a first switch connecting a power supply via the inductor to the gate and a second switch connected to the gate of the MOSFET for controlling a switching of the MOSFET are switched on.

Advantageously, this may provide for a fast and efficient, i.e. power

efficient operation of the MOSFET, allowing that such circuits may be applied to VRMs for data processors, SMPS for flat displays or SMPS for audio sets.

These and other aspects of the present invention will become apparent from and elucidated with reference to the embodiments described hereinafter.

Exemplary embodiments of the present invention will be described in the following, with reference to the following drawings:

Fig. 1 shows a simplified circuit diagram of a resonant gate driver circuit for driving a MOSFET.

Fig. 2 shows timing charts for explaining an operation of a resonant gate driver circuit.

Fig. 3 shows timing charts of an exemplary embodiment of a method of operating a resonant gate driver circuit according to the present invention.

Fig. 1 shows a circuit diagram of a resonant gate driver for driving a MOSFET 20, such as a power MOSFET, including a control circuit for operating the resonant gate driver circuit according to an exemplary embodiment of the present invention.

Reference numeral 2 in Fig. 1 designates a power supply generating a power supply voltage V_{CC}. Reference numeral 4 designates a first switch T_1 connected between the power supply voltage V_{CC} and a first end of an inductor 16. Reference numeral 6 designates a diode D_1. Reference numeral 10 designates a second switch T_2 connected between ground and the first end of the inductor L_1 16. Parallel to the switch T_2 10 between ground and the first end of the inductor L_1 16 there is provided another diode D_2 12. D_1 can be the intrinsic body diode of T_1 when T_1 is a MOSFET switch. D_2 can be the intrinsic body diode of T_2 when T_2 is a MOSFET switch. I_L is the current flowing into the inductor L_1 16.

Reference numeral 8 designates a third switch T_3 provided between the power supply voltage V_{CC} and a second end of the inductor L_1 16. The second end of

the inductor L_1 16 is also connected to a gate of the MOSFET 20. Reference numeral 14 designates a fourth switch T_4 provided between the second end of the inductor L_1 16 and ground. Between the second end of the inductor L_1 16, i.e. the gate of the MOSFET 20 and ground, parallel to the fourth switch T_4 14, there is drawn a capacitance C_{GS} 18. This may either be just the representation of the equivalent gate capacitance of the MOSFET 20, or it may be the sum of an external capacitance plus the representation of the equivalent gate capacitance of the MOSFET 20. A voltage across the capacitance C_{GS} 18 is referred to as V_{GS}.

Furthermore, according to an aspect of the present invention, there is provided a control circuit 22 for operating the switching of the first to fourth switches 4, 8, 10 and 14. The first to fourth switches $T_1$to T_4 (reference numerals 4, 8, 10 and 14). These may also be enhancement mode metal oxide semi-conductor field effect transistors (MOSFETs). However, it is also possible to, for example, to provide CMOS switches or other suitable switches. The control circuit may, for example, be realized by means of a state machine or EPLD, such as the ones manufactured by Alterra ® and maybe suitable switch drivers between the control circuit 22 and the respective one of the switches T_1 to T_4.

A drive signal provided from the control circuit 2 to the switches T_1 to T_4 may have a frequency extending from hundreds of KHz to the MHz range. The capacitance C_{GS} 18 may, depending on the frequency range where the circuit is operated, be in the range of 0,5 to 10nF and the inductor L_1 16 may have an inductance of 50-1000nH((e.g. 200nH for Cgs=2nF and 1MHz).

In the following, with reference to the timing charts of Fig. 2, an exemplary operation of the resonant gate driver circuit depicted in Fig. 1 will be described.

Timing chart 30 of Fig. 2 shows the switching of the first and second switches T1 and T2 over the time. The timing chart 32 of Fig. 2 shows the switching of the third and fourth switches T3 and T4 over the time. The timing chart 34 shows the corresponding I_L over the time and the timing chart 36 shows the voltage V_{GS} over the time.

As may be taken from Fig. 2, when the MOSFET 20 is to be switched on, the fourth switch T_4 switches off and at the same point in time t_1, the first switch T_1

switches on and connects the gate of the MOSFET 20 to V_{CC} via the inductor L_1 16. Vcc is provided by the power supply 2. This causes an increase of the inductor current I_L as shown in timing chart 34 until t_2 where the first switch T_1 is switched off and the third switch T_3 is switched on. At t_2, the inductor current I_L reaches its positive peak. At the same time t_2, the voltage V_{GS} reaches its desired value and the MOSFET 20 is fully switched on. After t_2, the energy recovery takes place via the diode D_2 and the third switch T_3, causing an almost linear decrease of the inductor voltage I_L. In practical applications, a diode parallel to T_3 can reduce the risk of over-voltage at the Vgs, which could result from improper timing. This over-voltage would reduce the efficiency of the converter and could sometimes even be destructive. This diode can be the intrinsic body diode of T_3 in case that T_3 is for example a MOSFET.

Thus, as may be taken from Fig. 2, it requires the time period $[t_1; t_2]$ until the full gate voltage of the MOSFET 20 is reached and the switching of the MOSFET 20 is complete. Thus, the inductor L_1, as may be taken from the timing chart 34, showing the inductor current I_L, slows the charge flow into the gate of the MOSFET 20 and therewith the rise of the gate voltage V_{GS} and thus the switching of the MOSFET 20.

At t_3, the third switch T_3 is switched off and the second switch T_2 is switched on. This causes an increase of the inductor current I_L, this time flowing in the direction opposite that during $[t_1; t_2]$. Due to this, from t_3 on the gate voltage V_{GS} decreases until it reaches zero at t_4, where the inductor current I_L reaches its peak and the second switch T_2 is switched off and the fourth switch T_4 is switched on. In practical applications, a diode parallel to T_4 can reduce the risk of negative over-voltage at the Vgs, which could result from improper timing. This over-voltage would reduce the efficiency of the converter and could sometimes even be destructive. This diode can be the intrinsic body diode of T_4 in case that T_4 is for example a MOSFET.

Thus, as may be taken from Fig. 2, it takes the time period between [t3; t4] until the gate voltage V_{GS} reaches zero and accordingly a relatively long time until the MOSFET 20 is switched off. Thus, in spite of the fact that such an operation is very loss efficient, it does not allow for the operation at high frequency, since the inductor L_1 slows down the rise and fall of the gate voltage V_{GS}.

Fig. 3 shows a method of operating the resonant gate driver circuit

according to the present invention, which, as indicated above, may be implemented with the control circuit 22 according to an exemplary embodiment of the present invention, controlling the first to fourth switches T_1 to T_4 to perform a switching as indicated in the timing charts 40 to 46 of Fig. 3. As indicated above, the control circuit may be implemented as a state machine or EPLD with suitable drivers to operate the first to fourth switches T_1 to T_4, as a digital circuit including amplifiers for driving the respective first to fourth switches T_1 to T_4 or may be realized as a suitable analogue circuit.

Timing chart 40 shows the switching of the first and second switches T_1 and T_2 over the time and timing chart 42 shows the switching of the third and fourth switches T_3 and T_4 over the time. The third timing chart 44 shows the inductor current I_L over the time and the fourth timing chart 46 shows the gate voltage across the capacitor C_{GS} 18 over the time.

As may be taken from Fig. 3, the first switch T_1 is switched on at t_5 before the fourth switch T_4 is switched off at t_6. This provides for an overlap time period, where both the first switch T_1 and the fourth switch T_4 are switched on. This causes a pre-charging of the inductor $L_1$16 as shown by I_L in the timing chart 44. In other words, before the fourth switch T_4 is switched off, controlling the switching of the MOSFET 20, the first switch T_1 is switched on, causing a pre-charging of the inductor $L_1$16. This pre-charging is realized by building up an inductor current during $[t_5; t_6]$ before the actual switching of the MOSFET 20, which follows at t_6 by shutting the fourth transistor T4 off.

In other words, the pre-charging of the inductor $L_1$16 is performed by providing an overlap time period, during which the first switch T_1 and the fourth switch T_4 are switched on.

Then, after the switching of the fourth switch T_4 at t_6, the inductor current I_L increases up to its peak at t_7, where the first switch T_1 is shut off and the gate voltage V_{gs} reaches its desired level.

As a comparison of $[t_1; t_2]$ to $[t_6; t_7]$ shows, the time period $[t_6; t_7]$ is significantly shorter than the time period $[t_1; t_2]$. Thus, according to the exemplary embodiment of the present invention shown in Fig. 3, the actual switching time required for switching the MOSFET 20 can be reduced significantly. As described above, this is

done by providing an overlap time of the first switch T_1 and the fourth switch T_4. Due to this, the inductor current I_L is built up, starting at t_5 previous to the switching action at t_6. Due to this, in comparison to Fig. 2, a much higher initial current charges the gate, which allows for a much faster charging of the gate capacitance C_{gs}18.

Advantageously, by performing the switching operation as described with reference to Fig. 3, a very efficient switching may be performed, even at high switching frequencies. Also, as a comparison of V_{GS} of a timing chart 36 in Fig. 2 to the timing chart 46 in Fig. 3 shows, the voltage slope between t_6 and t_7 is significantly steeper than the voltage slope between t_1 and t_2.

At t_8, the second switch T_2 is switched on before the third switch T_3 is switched off at t_9. This provides for an overlap time period from t_8 to t_9, where the second transistor T_2 connecting the gate of the MOSFET 20 via the inductor L_1 16 to ground (- of the power supply 2) and the third switch T_3 controlling the switching of the MOSFET 20 being connected to the gate of the MOSFET 20, are switched on. By this, the inductor L_1 16 is pre-charged by building up the inductor current I_L. Then, at t_9, the third transistor T3 is switched off. This causes a sharp decrease of the gate voltage V_{GS} as may be taken from the timing chart 46. Furthermore, this causes a further charging of the inductor $L_1$16 until t_{10} where the second transistor T_2 is shut off, the fourth transistor T_4 is switched on, the inductor current I_L reaches its peak and the gate voltage V_{GS} is down to ground. Then, after t_{10}, the inductor current I_L almost linearly drops to zero, as may be taken from the timing chart 44.

As a comparison of the time period [t_9; t_{10}] to the time period [t_3; t_4] of the timing chart 36 in Fig. 2 shows, the time period [t_9; t_c] is significantly shorter than the time period [t_3; t_4]. Thus the voltage drop of the voltage V_{GS} during [t_9; t_{10}] is significantly steeper than during [t_3; t_4].

As may be taken from Fig. 3, a very fast and efficient switching (off switching) may be achieved by providing an overlap time between the second switch T_2 and the third transistor T_3. By this, an inductor current I_L is built up during [t_8; t_9] prior to the switching action at t_9. Due to this a much higher initial current I_L charges the gate of the MOSFET 20, which allows for a much faster charging of the gate capacitors C_{GS}18.

According to an aspect of the present invention, the pre-charging is

performed such that the inductor current I_L reaches approximately half of its peak-value before the switching of the respective one of switches T_3 and T_4 controlling the switching of MOSFET 20.

Thus, as described above, a method of operating a resonant gate driver circuit for driving a MOSFET and a control circuit for controlling the switches of a resonant gate driver circuit according to exemplary embodiments of the present invention are provided, allowing for a combination of fast switching and very high efficiency. Advantageously, this may allow the application of resonant gate driver circuit in, for example, power electronics with MOSFETs which work with high switching frequencies. Those may, for example, advantageously be used in SMPS with special requirements, such as flatness, size EMI or dynamics. Exemplary application fields are, for example, VRMs for data processors, SMPS for flat displays or SMPS for audio sets.

Instead of MOSFETs as used in the above exemplary embodiments, the present invention is also applicable for almost all kinds of voltage controlled semiconductor switches such as IGBTs. Furthermore, the present invention may be applied to current controlled semiconductors such as bipolar transistors, thyristors and triacs.